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Versatile Unified Power Quality Conditioner Applied to Three-Phase Four-Wire Distribution Systems Using a Dual Control Strategy

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***Abstract*— This paper presents the study, analysis and practical implementation of a versatile unified power quality conditioner (UPQC), which can be connected in both three-phase three-wire or three-phase four-wire distribution systems for performing the series-parallel power-line conditioning. Thus, even when only a three-phase three-wire power system is available at a plant site, the UPQC is able to carry out power-line compensation for installed loads that require a neutral conductor to operate. Different from the control strategies used in the most of UPQC applications in which the controlled quantities are non-sinusoidal, this UPQC employs a dual compensation strategy, such that the controlled quantities are always sinusoidal. Thereby, the series converter is controlled to act as a sinusoidal current source, whereas the parallel converter operates as a sinusoidal voltage source. Thus, because the controlled quantities are sinusoidal, it is possible to reduce the complexity of the algorithms used to calculate the compensation references. Therefore, since the voltage and current controllers are implemented into the synchronous reference frame, their control references are continuous, decreasing the steady-state errors when traditional proportional-integral controllers are employed. Static and dynamic performances, as well as the effectiveness of the dual UPQC are evaluated by means of experimental results.**

***Index Terms*— Active filter, dual control strategy, power conditioning, three-phase distribution systems, UPQC.**

I. Introduction

THE demand for power quality (PQ) improvement has been growing in recent years, mainly due to the increase of nonlinear loads connected to the electrical power system causing distortions in the utility voltages at the point of common coupling. Other PQ problems, such as voltage sags/swells and voltage unbalances can also affect the proper operation of sensitive equipment causing malfunction. Furthermore, additional procedures should be taken into account in order to overcome PQ problems associated with harmonic currents generated by nonlinear loads, load unbalances and reactive power demanded by the load.

Several procedures have been adopted to mitigate PQ problems, which can be carried out by means of active power-line conditioners, such as unified power quality conditioners (UPQCs) [1]-[17], shunt [18]-[24], series [25] and hybrid active power filters (APFs) [26], [27] and dynamic voltage restorers [28].

By means of single-phase [18], [19] or three-phase [20]-[24] topologies, shunt APFs are placed in parallel with non-linear loads, and controlled to operate as a non-sinusoidal current source. In three-phase systems, they can only be employed for compensating harmonic currents [20] or load unbalances and load reactive power compensation [21]-[24]. Operating as non-sinusoidal voltage sources [26] or sinusoidal current sources [27], series APF filters, which are placed between the utility grid and the load, can compensate harmonic currents, load unbalances and reactive power of the load, while the load voltages are regulated [27]. On the other hand, UPQC systems can perform, simultaneously, the series-parallel active power-line compensation by using both series and parallel APFs. Thus, for overcoming utility PQ problems, UPQCs have been employed based on different concepts and solutions [10], [13], [15], comprising single-phase systems [14] or in three-phase applications, considering three-phase three-wire (3P3W) systems [1], [3], [9], [17] or three-phase four-wire (3P4W) systems [2], [4], [8], [11], [12]. Accordingly, in most UPQC-based applications, the series and parallel APFs are controlled as non-sinusoidal sources by using non-sinusoidal references to control voltage and current quantities [1], [6]-[17].

It is well known that non-sinusoidal references are difficult to be synthesized by PWM converters and require an additional effort in order to achieve good performance in APF or UPQC applications. On the other hand, sinusoidal control references have been used in applications involving uninterruptible power supply (UPS) systems [29], [30], such that in the standby operation mode the UPS system acts similarly to a UPQC performing the series-parallel power compensation. In this application, the series converter is controlled to operate as a sinusoidal current source rather than a non-sinusoidal voltage source, while in the parallel conditioning the parallel converter is controlled to operate as a

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sinusoidal voltage source rather than a non-sinusoidal current source.

In addition, this dual compensation strategy has also been tested in UPQC applications [2]-[4]. Thus, different from the conventional conditioning strategy, which uses non-sinusoidal control references, the dual compensating strategy uses only sinusoidal references to control the PWM converters. As a result, the generation of the control references is easier to obtain, allowing the use of simpler algorithms to accomplish this aim.

It can be noted that, since the parallel converter is controlled to handle only sinusoidal voltages [2], [3], [29], [30], the utility voltage components that are different from the positive sequence components will appear across the series coupling transformers, so that they are indirectly compensated without the need to calculate any non-sinusoidal compensation reference voltages. Moreover, since the output voltages are controlled to be in phase with the utility voltages, the use of a Phase-locked Loop (PLL) system operating with constant amplitude is necessary in order to generate the sinusoidal output voltage references.

Synchronous Reference Frame (SRF) based controllers (*dq0*-axes) are implemented in this paper to control the input currents and the output voltages of the UPQC. Due to the voltage and current references being sinusoidal, the use of continuous control references into the SRF-based controllers is allowed, leading to a reduction in steady-state errors when conventional Proportional-Integral (PI) controllers are chosen to be implemented in this same reference frame, representing another important advantage when the dual compensation strategy is compared to the conventional one.

The UPQC input currents are also controlled to be in phase with the utility voltages. Thereby, the estimated utility phase-angle (θ) obtained from the PLL is also employed to generate the sinusoidal input current references. In addition, θ is used for obtaining the coordinates of the unit vector ($sin\,\theta$ and $cos\,\theta$) of the SRF-based controllers. In this paper, a three-phase power-based PLL (3pPLL) scheme is employed [9], [30]. Once the conventional 3pPLL suffers with utility voltage disturbances, such as harmonics and/or unbalances, a self-tuning filter (STF) [23] is used in conjunction with the 3pPLL scheme. The STF is placed between the utility voltages and the 3pPLL scheme, where the angular frequency estimated from the 3pPLL is used to adjust the STF cut-off frequency, avoiding that variations in utility frequency can interfere or affect its performance.

The main contribution of this paper is to present the practical implementation of a 3P4W distribution system based on UPQC topology, which has been previously evaluated in [6] using simulations. This versatile UPQC topology can be connected either in three-phase three-wire (3P3W) or in three-phase four-wire (3P4W) distribution power systems, to perform active power-line conditioning. Nevertheless, its main application is indicated for 3P3W systems. Thus, if only a 3P3W power supply system is available at a plant site, the implemented UPQC is able to perform the power-line compensation even when the installed single-phase loads require the neutral conductor to operate.

In [6], the effectiveness of the UPQC-based 3P4W distribution system was evaluated only by means of simulation results, in which the well-known strategy based on the *p-q* theory [33] was used to obtain the compensation references of voltages and currents. Besides the experimental results used to evaluate the static and dynamic performance, as well as the effectiveness of the UPQC topology, this paper aims to employ the dual compensating strategy implementation, with its inherent advantages, to achieve the following purposes: i) suppress load harmonic currents; ii) compensate load reactive power; iii) compensate load unbalances; iv) compensate utility voltage unbalances; v) suppress utility harmonic voltages; and vi) regulate the output voltages.

This paper is organized as follows: Section II describes the structure of the UPQC topology and its main features are highlighted. Section III presents the state feedback of the current and voltage controllers, while the stability analysis is treated in Section IV. The strategies used to generate the sinusoidal references of voltages and currents are presented in Section V. In Section VI the static and dynamic performances of the UPQC are evaluated by means of experimental tests. Finally, Section VII presents the conclusions of the paper.

II. UPQC Topology Description

The UPQC topology employed to implement the dual compensation strategy presented in this paper is shown in Fig. 1. It is comprised of both Three-Leg (3-Leg) and Four-Leg (4-Leg) PWM converters sharing the same DC-link.

The UPQC is connected between a 3P3W power supply distribution system and a 3P4W plant site composed of several types of three-phase and single-phase loads. It is assumed that the single-phase loads use the neutral conductor to operate. In this case, a 3P4W distribution system is necessary, which is composed of three power conductors and a neutral conductor to feed the loads. Thus, as can be noted in the UPQC-based 3P4W distribution system shown in Fig. 1, the neutral current flows through the wire conductor connected to the fourth leg of the shunt 4-Leg PWM converter.

The 4-Leg PWM converter [6], [8], [12] was chosen to act as the shunt APF, because it is able to operate with lower DC-link voltage amplitude when compared to the 3-Leg PWM split-capacitor topology [2], [15]. In addition, the 3-Leg split-capacitor topology requires an additional control loop to compensate its inherent DC-link capacitor voltage unbalances. Although the 4-Leg converter has a greater number of switches, the power rating of the devices that compose its fourth leg is reduced, because the current that flows through the neutral conductor in most cases is low.

A. Dual Compensation Principle

In order to make the input currents sinusoidal, balanced and in phase with the utility voltages, in the dual compensating strategy, the series PWM converter is controlled to operate as a sinusoidal current source. In this case, its impedance must be high enough to isolate the harmonic currents generated by the non-linear loads. On the other hand, the parallel PWM converter also makes the output voltages sinusoidal, balanced, regulated and in phase with the utility voltages. In other words, it is controlled to operate as a sinusoidal voltage source, such that its impedance must be sufficiently low to absorb the load harmonic currents [30].

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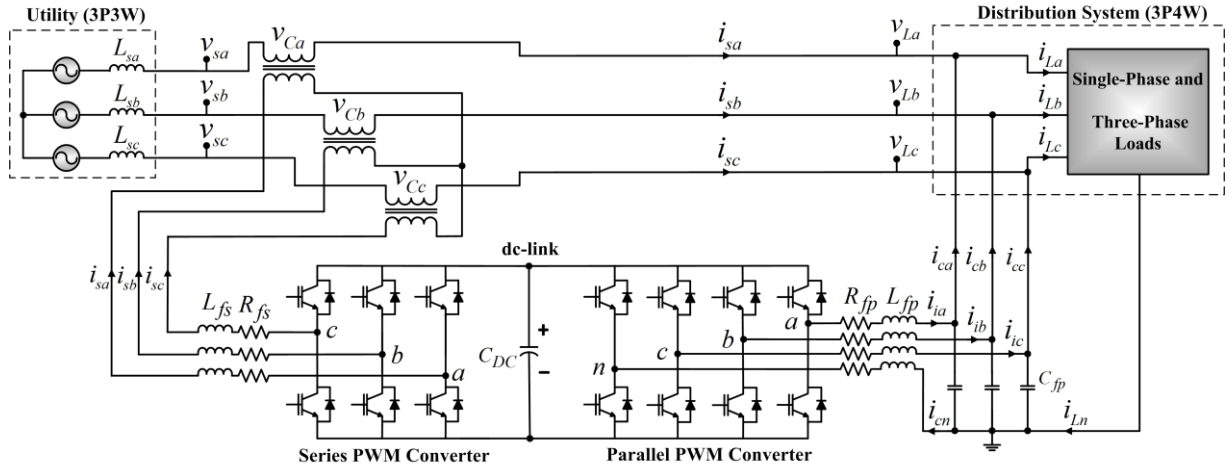

Fig. 1. 3P4W distribution system based on UPQC topology connected to 3P3W power system.

Since the series and parallel converters have high and low impedances, respectively, the load harmonic currents flow naturally through the parallel converter. Furthermore, compensation for load unbalances is ensured by controlling the series converter to follow sinusoidal and balanced references so that the negative and zero sequence components are compensated. Finally, the fundamental reactive power compensation is ensured by controlling the series converter current references to be in phase with the utility voltages.

On the other hand, the utility harmonic voltages and unbalances are compensated ensuring that the controlled output voltages follow sinusoidal and balanced references, such that the amplitude differences between the input and output voltages will appear across the series coupling transformers, meaning that any utility voltage disturbances are naturally compensated. This makes the dual compensating strategy more attractive than the conventional strategy, considering that the load is less affected by the occurrence of grid voltage disturbances, such as voltage sags. This is possible because, different from the conventional strategy in which the series converter controls the output voltages, in the dual compensating strategy this task is entirely assumed by the parallel converter.

III. Modeling of Series and Parallel Converters

The modeling of the series and parallel PWM converters are presented in this section. In addition, the voltage and current controllers implemented in the SRF *(dq0*-axes*)* are discussed.

A. Series Converter Modeling

The state-space system and the transfer functions of the series converter in the *dq*-axes are obtained based on a mathematical model. The modeling is accomplished considering that all involved inductances and resistances are identical, as follows: $L_{fsa} = L_{fsb} = L_{fsc} = L_{fs}$ and $R_{fsa} = R_{fsb} = R_{fsc} = R_{fs}$. By means of Fig. 1, the equations that represent the system are given by (1) and (2).

$$u_{sab\_pwm} = v_{Lfsa} + v_{Rfsa} + v_{Cab} - v_{Rfsb} - v_{Lfsb} \quad (1)$$

$$u_{sbc\_pwm} = v_{Lfsb} + v_{Rfsb} + v_{Cbc} - v_{Rfsc} - v_{Lfsc} \quad (2)$$

where: u_{sab_pwm} and u_{sbc_pwm} are the respective PWM voltages at the 3-Leg series converter terminals.

Considering the voltages of the PWM series converter in the *dq*-axes (u_{sd_pwm} and u_{sq_pwm}), the state-space equation is given by:

$$\dot{x}_{sdq}(t) = A_{sdq}.x_{sdq}(t) + B_{sdq}.u_{sdq}(t) + F_{sdq}.w_{sdq}(t) \quad (3)$$

where:

$$\dot{x}_{sdq}(t) = \begin{bmatrix} \frac{di_{sd}}{dt} \\ \frac{di_{sq}}{dt} \end{bmatrix}; \; x_{sdq}(t) = \begin{bmatrix} i_{sd} \\ i_{sq} \end{bmatrix}; \; u_{sdq} = \begin{bmatrix} u_{sd\_pwm} \\ u_{sq\_pwm} \end{bmatrix};$$

$$w_{sdq}(t) = \begin{bmatrix} v_{Cd} \\ v_{Cq} \end{bmatrix}; \; A_{sdq} = \begin{bmatrix} -\frac{R_{fs}}{L_{fs}} & \omega \\ -\omega & -\frac{R_{fs}}{L_{fs}} \end{bmatrix}; \; B_{sdq} = \frac{1}{3L_{fs}} \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix};$$

$$F_{sdq} = \frac{1}{3L_{fs}} \begin{bmatrix} -1 & 0 \\ 0 & -1 \end{bmatrix}.$$

Thereby, based on (3), the series converter average model represented as a signal flow graph is shown in the dotted area of Fig. 2(a). In addition, the current controller into the *dq*-axes is also shown, where $Gs_{(PI)d}$ and $Gs_{(PI)q}$ represent the transfer functions of the PI current controllers; D_{sd} and D_{sq} are the duty cycles; V_{DC} is the DC-bus voltage; and K_{PWM} is the gain of the PWM modulator given by $K_{PWM} = 1/P_{PWM}$ [31], where P_{PWM} is the peak value of the PWM triangular carrier implemented in the digital signal processor (DSP). The current coupling between the *dq*-axes, shown in the average model of Fig. 2(a), is eliminated by using the scheme presented in Fig. 2(b), where the dotted blocks represent the decoupling effects [32] implemented in the block diagram shown in Fig. 2(a).

Thus, based on Fig. 2(a), the transfer functions of the closed loop system can be represented by (4), where $Kp_{s(d,q)}$ and $Ki_{s(d,q)}$ are the proportional and integral controller gains, and $i^*_{s(d,q)}(s)$ represents the continuous current references in the *dq* coordinates.

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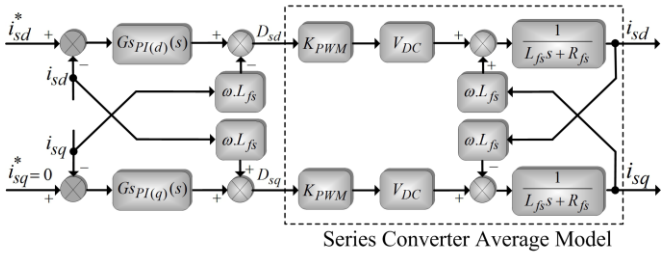
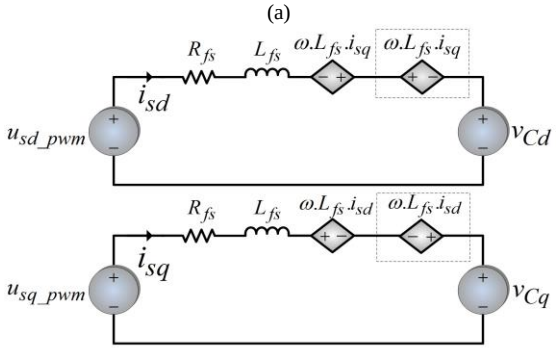
$$\frac{i_{S(d,q)}(s)}{i^*_{S(d,q)}(s)} = \frac{X_1(Kp_{s(d,q)}s + Ki_{s(d,q)})}{L_{fs}s^2 + (R_{fs} + X_1 Kp_{s(d,q)})s + X_1 Ki_{s(d,q)}} \quad (4)$$

where: $X_1 = K_{PWM}V_{DC}$



(a)



(b)

Fig. 2. Series converter: (a) Signal flow graph of the current controllers and average model; (b) Model of the uncoupled system in SRF *dq*-axes.

B. Parallel Converter Modeling

The state-space system and the transfer functions of the parallel converter in the *dq0*-axes are obtained based on a mathematical model. The modeling is accomplished considering that all involved inductances, resistances and capacitances are identical, as follows: $L_{fpa} = L_{fpb} = L_{fpc} = L_{fpn} = L_{fP}$; $R_{fpa} = R_{fpb} = R_{fpc} = R_{fpn} = R_{fp}$, and $C_{fpa} = C_{fpb} = C_{fpc} = C_{fp}$.

By means of Fig. 1, the equations that represent the system are given by (5), (6) and (7), as follows:

$$u_{pan\_pwm} = R_{fpa}.i_{ia} + L_{fpa}\frac{di_{ia}}{dt} + v_{La} + L_{fpn}\frac{di_{cn}}{dt} + R_{fpn}.i_{cn} \quad (5)$$

$$u_{pbn\_pwm} = R_{fpb}.i_{ib} + L_{fpb}\frac{di_{ib}}{dt} + v_{Lb} + L_{fpn}\frac{di_{Cn}}{dt} + R_{fpn}.i_{cn} \quad (6)$$

$$u_{pcn\_pwm} = R_{fpc}.i_{ic} + L_{fcc}\frac{di_{ic}}{dt} + v_{Lc} + L_{fpn}\frac{di_{Cn}}{dt} + R_{fpn}.i_{cn} \quad (7)$$

where: u_{pan_pwm}, u_{pbn_pwm}, and u_{pcn_pwm} are the respective PWM voltages at the terminals *a*, *b* and *c* of the 4-L parallel converter.

The capacitor currents of the output filters (i_{Cfpa}, i_{Cfpb}, and i_{Cfpc}) are given by:

$$i_{Cfpa} = C_{fpa}\frac{dv_{La}}{dt} = i_{ia} - i_{ca} \quad (8)$$

$$i_{Cfpb} = C_{fpb}\frac{dv_{Lb}}{dt} = i_{ib} - i_{cb} \quad (9)$$

$$i_{Cfpc} = C_{fpc}\frac{dv_{Lc}}{dt} = i_{ic} - i_{cc} \quad (10)$$

where i_{ia}, i_{ib} and i_{ic} are the currents of the inductors, and i_{ca}, i_{cb} and i_{cc} are the output currents of the parallel converter.

Considering the PWM converter voltages of the parallel synchronous rotating frame (u_{pd_pwm}, u_{pq_pwm}, and u_{p0_pwm}), the state-space equation is found as:

$$\dot{x}_{pdq0}(t) = A_{pdq0}.x_{pdq0}(t) + B_{pdq0}.u_{pdq0}(t) + F_{pdq0}.w_{pdq0}(t) \quad (11)$$

where:

$$\dot{x}_{pdq0}(t) = \left[\frac{di_{id}}{\mathrm{dt}} \quad \frac{di_{iq}}{\mathrm{dt}} \quad \frac{di_{i0}}{\mathrm{dt}} \quad \frac{dv_{Ld}}{\mathrm{dt}} \quad \frac{dv_{Lq}}{\mathrm{dt}} \quad \frac{dv_{L0}}{\mathrm{dt}}\right]^T;$$

$$x_{pdq0}(t) = [i_{id} \quad i_{iq} \quad i_{i0} \quad v_{Ld} \quad v_{Lq} \quad v_{L0}]^T;$$

$$u_{pdq0}\begin{bmatrix} u_{pd\_pwm} \\ u_{pq\_pwm} \\ u_{p0\_pwm} \end{bmatrix};\ w_{pdq0}\begin{bmatrix} i_{Cfpd} \\ i_{Cfpq} \\ i_{Cfp0} \end{bmatrix};$$

$$A_{pdq0} = \begin{bmatrix} -\frac{R_{fp}}{L_{fp}} & \omega & 0 & -\frac{1}{L_{fp}} & 0 & 0 \\ -\omega & -\frac{R_{fp}}{L_{fp}} & 0 & 0 & -\frac{1}{L_{fp}} & 0 \\ 0 & 0 & -\frac{R_{fp}}{L_{fp}} & 0 & 0 & -\frac{1}{4L_{fp}} \\ \frac{1}{C_{fp}} & 0 & 0 & 0 & \omega & 0 \\ 0 & \frac{1}{C_{fp}} & 0 & -\omega & 0 & 0 \\ 0 & 0 & \frac{1}{C_{fp}} & 0 & 0 & 0 \end{bmatrix};$$

$$B_{pdq0} = \begin{bmatrix} \frac{1}{L_{fp}} & 0 & 0 \\ 0 & \frac{1}{L_{fp}} & 0 \\ 0 & 0 & \frac{1}{4L_{fp}} \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix};\ F_{pdq0} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ -\frac{1}{C_{fp}} & 0 & 0 \\ 0 & -\frac{1}{C_{fp}} & 0 \\ 0 & 0 & -\frac{1}{C_{fp}} \end{bmatrix}.$$

Thereby, based on (11), the parallel converter average model represented as a signal flow graph is shown in the dotted area of Fig. 3(a). In addition, the voltage and current controllers into the *dq0*-axes are presented, where $Gp_{PIv(d)}$, $Gp_{PIv(q)}$ and $Gp_{PIv(0)}$ represent the transfer functions of the PI voltage controllers (outer loops); $Gp_{Pi(d)}$, $Gp_{Pi(q)}$ and $Gp_{Pi(0)}$ are the transfer functions of the proportional current controllers (inner loops); and D_{pd}, D_{pq} and D_{p0} are the duty cycles. The current and voltage coupling between the *dq*-axes shown in the average model of Fig. 3(a) is eliminated by using the scheme presented in Fig. 3(b), where the dotted blocks represent the decoupling effects, which are implemented in the block diagram shown in Fig. 3(a).

Thus, based on Fig. 3(a), the transfer functions of the closed loop system can be represented by (12) and (13), where $Kp_{p(d,q)}$, $Ki_{p(d,q)}$ and $Ki_{p(0)}$ are the proportional and integral gains of the controllers (outer voltage control loop), $Kp_{pi(d,q)}$ and $Kp_{pi(0)}$ are the proportional gains (inner current control loop), and $v^*_{L(d,q,0)}(s)$ represents the continuous voltage references in the *dq0* coordinates.

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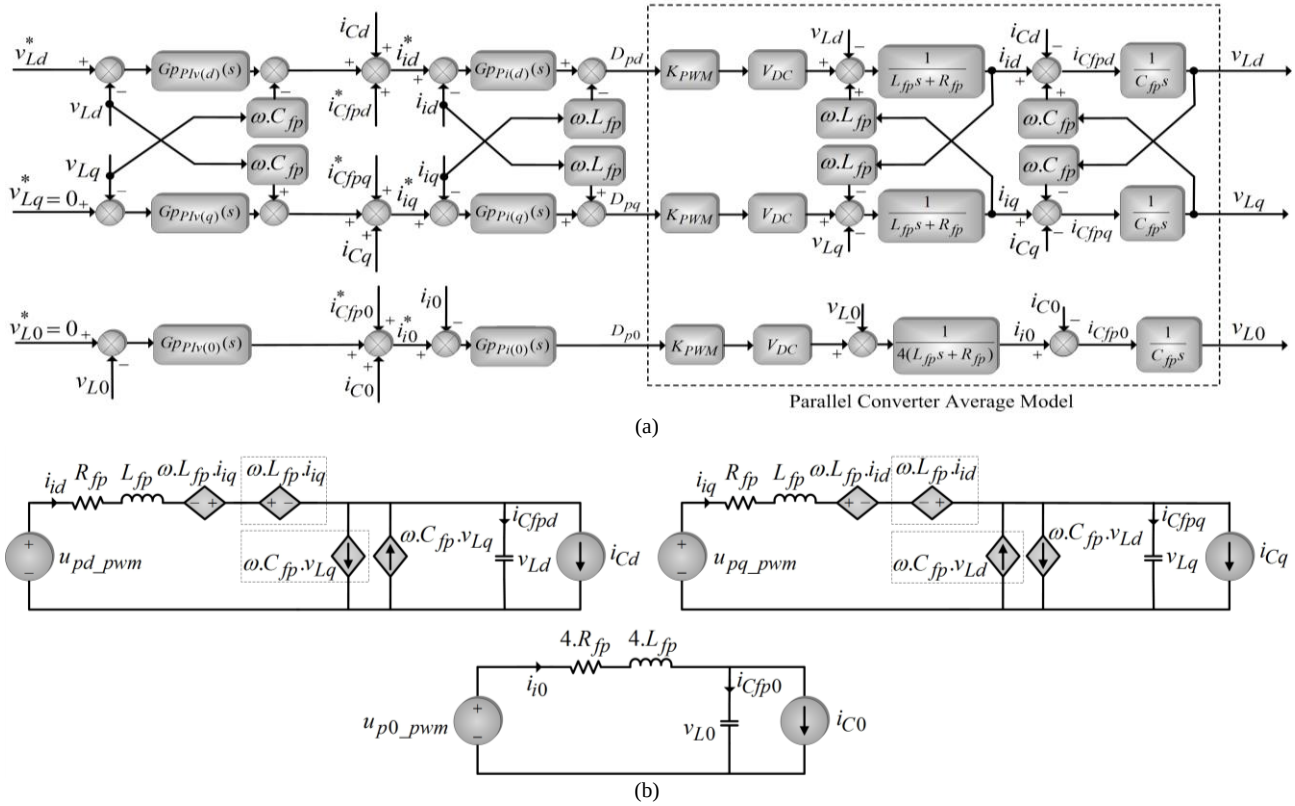

Fig. 3. Parallel converter: (a) Signal flow graph of the voltage controllers and average model; (b) Model of the uncoupled system in SRF *dq0*-axes.

The currents of the filter capacitors $i_{Cfp(d,q,0)}$ shown in Fig. 3(a) are estimated considering the derivatives of the measured output voltages $(v_{La,b,c})$ and the respective capacitances $(C_{fpa,b,c})$ [4].

$$\frac{v_{L(d,q)}(s)}{v^*_{L(d,q)}(s)} = \frac{X_{1(d,q)}s^2 + X_{2(d,q)}s + X_{3(d,q)}}{Y_{1(d,q)}s^3 + Y_{2(d,q)}s^2 + Y_{3(d,q)}s + Y_{4(d,q)}} \quad (12)$$

$$\frac{v_{L(0)}(s)}{v^*_{L(0)}(s)} = \frac{X_{1(0)}s^2 + X_{2(0)}s + X_{3(0)}}{Y_{1(0)}s^3 + Y_{2(0)}s^2 + Y_{3(0)}s + Y_{4(0)}} \quad (13)$$

where:

$X_{1(d,q)} = K_{PWM}V_{DC}C_{fp}Kp_{pi(d,q)}$;
$X_{2(d,q)} = K_{PWM}V_{DC}Kp_{pi(d,q)}Kp_{p(d,q)}$;
$X_{3(d,q)} = Y_{4(d,q)} = K_{PWM}V_{DC}Kp_{pi(d,q)}Ki_{p(d,q)}$;
$Y_{1(d,q)} = C_{fp}L_{fp}$;
$Y_{2(d,q)} = C_{fp}(K_{PWM}V_{DC}Kp_{pi(d,q)} + R_{fp})$;
$Y_{3(d,q)} = K_{PWM}V_{DC}Kp_{pi(d,q)}Kp_{p(d,q)} + 1$;
$X_{1(0)} = K_{PWM}V_{DC}C_{fp}Kp_{pi(0)}$;
$X_{2(0)} = K_{PWM}V_{DC}Kp_{pi(0)}Kp_{p(0)}$;
$X_{3(0)} = Y_{4(0)} = K_{PWM}V_{DC}Kp_{pi(0)}Ki_{p(0)}$;
$Y_{1(0)} = 4C_{fp}L_{fp}$;
$Y_{2(0)} = C_{fp}(K_{PWM}V_{DC}Kp_{pi(0)} + 4R_{fp})$;
$Y_{3(0)} = K_{PWM}V_{DC}Kp_{pi(0)}Kp_{p(0)} + 4$.

IV. Stability Analysis of the System

This section presents the stability study of the UPQC system, which involves the series and parallel converters. The aim of this study was to verify the ability of the system to remain stable even under load disturbances.

A. Series APF

Considering the signal flow graph of the current controller and the series converter average model shown in Fig. 2(a), the closed loop transfer function in the *dq* coordinates can be represented by (4). Thereby, the stability analysis of the series converter involves only the second order denominator (λ_i) of (4). By applying the Routh-Hurwitz stability criterion, the necessary and sufficient conditions for ensuring the series converter stability is that all the coefficients of λ_i must have the same sign. As can be noted, all the coefficients are positive, meaning that the series converter control is always stable. In addition, load transients only affect the generation of the series current references. Therefore, since the reference currents are always sinusoidal, it is possible to assume that the series converter remains acting as a sinusoidal current source even when load transients occur.

B. Parallel APF

Considering the signal flow graph of the voltage controllers and the parallel converter average model shown in Fig. 3(a), the closed loop transfer functions in the *dq0* coordinates can be represented by (12) and (13). Considering that the PI controller gains $Kp_{pi} = Kp_{pi(d,q)} = Kp_{pi(0)}/4$; $Kp_p = Kp_{p(d,q)} = Kp_{p(0)}$ and $Ki_p = Ki_{p(d,q)} = Ki_{p(0)}$, the same transfer function is obtained for each control loop implemented in the *d*, *q* and *0* coordinates as given by (14), allowing the study of the voltage control loops by means of a unique transfer function $G_v(s)$. In addition, it is assumed that the individual control loops in the *dq0* coordinates are obtained taking into account the coupling effects between the *dq* coordinates shown in Fig. 3.

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$$G_v(s) = \frac{v_{L(d,q,0)}(s)}{v^*_{L(d,q,0)}(s)} = \frac{(1+K)\left[X_{1(d,q,0)}s^2 + X_{2(d,q,0)}s + X_{3(d,q,0)}\right]}{Y_{1(d,q,0)}s^3 + Y_{2(d,q,0)}s^2 + Y_{3(d,q,0)}s + Y_{4(d,q,0)}} \quad (14)$$

where:

$X_{1(d,q,0)} = K_{PWM}V_{DC}C_{fp}Kp_{pi}$;
$X_{2(d,q,0)} = K_{PWM}V_{DC}Kp_{pi}Kp_p$;
$X_{3(d,q,0)} = Y_{4(d,q,0)} = K_{PWM}V_{DC}Kp_{pi}Ki_p$;
$Y_{1(d,q,0)} = C_{fp}L_{fp}$;
$Y_{2(d,q,0)} = C_{fp}(K_{PWM}V_{DC}Kp_{pi} + R_{fp})$;
$Y_{3(d,q,0)} = K_{PWM}V_{DC}Kp_{pi}Kp_p + 1$.

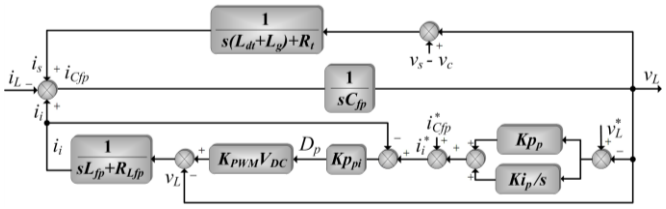

Fig. 4. Parallel converter equivalent model used to stability analysis for the *dq0* voltage control loops.

However, it is not possible to analyze how the load current transients will interfere in the controls of the UPQC output voltages only by using the transfer function G_v(s). Thus, Fig. 4 presents the block diagram, which is based on the control loops shown in Fig. 3(a), as well as the aforementioned considerations. Thus, the load current (i_L) is considered as an input of the system, whereas the voltage (v_L) is the output. In addition, in order to obtain an adequate representation of the system, the source current (i_s) is calculated from both the output voltage (v_L) and input voltage (v_s), taking into account the leakage inductances and resistances of the series coupling transformers (L_{dt} and R_t), as well as the grid equivalent inductances (L_g). Thereby, from Fig. 4, the closed loop transfer function $G_{iv}(s) = v_{L(d,q,0)}(s)/i_{L(d,q,0)}(s)$ can be obtained by (15). By applying the Routh-Hurwitz stability criterion, two conditions must be met: i) all the polynomial coefficients of the denominator must have the same sign; ii) the inequality $Y_2Y_3 > Y_1Y_4$ must be respected. Therefore, by inspecting the denominator of (15), the first condition is always met. On the other hand, the second condition can be met by adjusting the PI controller gains. Thus, taking into account the aforementioned conditions, the system will always be stable, even when load transients occur.

$$G_{vi}(s) = \frac{v_{L(d,q,0)}(s)}{i_{L(d,q,0)}(s)} = \frac{X_1s^2 + X_2s + X_3}{Y_1s^3 + Y_2s^2 + Y_3s + Y_4} \quad (15)$$

where:

$K = K_{PWM}V_{DC}Kp_{pi}$;
$X_1 = (L_{dt} + L_s)L_{fp}$;
$X_2 = (L_{dt} + L_s)R_{Lfp} + L_{fp}R_t$;
$X_3 = R_tR_{L_{fp}}$;
$Y_1 = C_{fp}L_{fp}(L_{dt} + L_s)$;
$Y_2 = C_{fp}(L_{dt} + L_s)R_{L_{fp}} + C_{fp}L_{fp}R_t + C_{fp}(L_{dt} + L_s)K + Kp_pK$;
$Y_3 = C_{fp}R_tR_{L_{fp}} + C_{fp}R_tK + Kp_pR_{L_{fp}}K + L_{fp}Ki_pK + (L_{dt} + L_s)$;
$Y_4 = R_{L_{fp}} + R_{L_{fp}}Ki_pK + K$.

V. Control References of the Series and Parallel Converters

In this section the strategies used to generate the sinusoidal reference quantities used to control the series and the parallel converters are presented. As aforementioned, both the current and voltage control references are controlled to be in phase with the utility voltages. Since the controlled voltages and currents are sinusoidal quantities, a significant advantage is attained when the dual compensating strategy is compared with the conventional strategy, whose controlled quantities are always non-sinusoidal. This advantage is highlighted mainly because the control references into the SRF-based controllers are continuous, leading to reduced errors in the steady-state of the PI controllers.

A. Series Converter Reference Currents

The current control loop of the series converter is shown in the signal flow graph of Fig. 5(a). The continuous reference current in the SRF direct axis *d* is defined by i^*_{sd}, which is able to make the serial converter synthesize the sinusoidal input currents (i_{sa}, i_{sb}, i_{sc}). As can be noted, the three-dimensional space vector modulation (3-D-SVM) technique is used in the series converter.

The reference current i^*_{sd} is obtained by measuring the load currents (i_{La}, i_{Lb}, i_{Lc}) and converting them to the rotating reference frame. Thus, the direct current (i_d) is achieved by means of (16) and (17), whereas the utility phase-angle θ, used to calculate the coordinates of the unit vectors $sin\,\theta$ and $cos\,\theta$, is obtained from the three-phase PLL system. Next, a low-pass filter (LPF) is employed to obtain the direct component ($i_{d_{dc}}$), which represents, in the SRF, the active portions of the load currents (i_{La}, i_{Lb}, i_{Lc}). In other words, $i_{d_{dc}}$ represents the positive sequence components of the load currents.

$$\begin{bmatrix} i_\alpha \\ i_\beta \\ i_0 \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \quad (16)$$

$$i_d = i_\alpha cos\theta + i_\beta sin\theta \quad (17)$$

The control of the power balance flow through the UPQC must be take into account in order to maintain the DC-bus voltage constant. Thereby, the final reference current i^*_{sd} is calculated by using (18), where i_{dc} is added to $i_{d_{dc}}$. Thus, i_{dc} represents the control action of the DC-bus voltage controller that compensates the inherent losses of the filter elements and semiconductor devices. In addition, i_{dc} controls the balance of the power flow through the UPQC when different amplitudes between the input voltages (v_{sa}, v_{sb}, v_{sc}) and output voltages (v_{La}, v_{Lb}, v_{Lc}) occur [30].

$$i^*_{sd} = i_{dc} + i_{d_{dc}} \quad (18)$$

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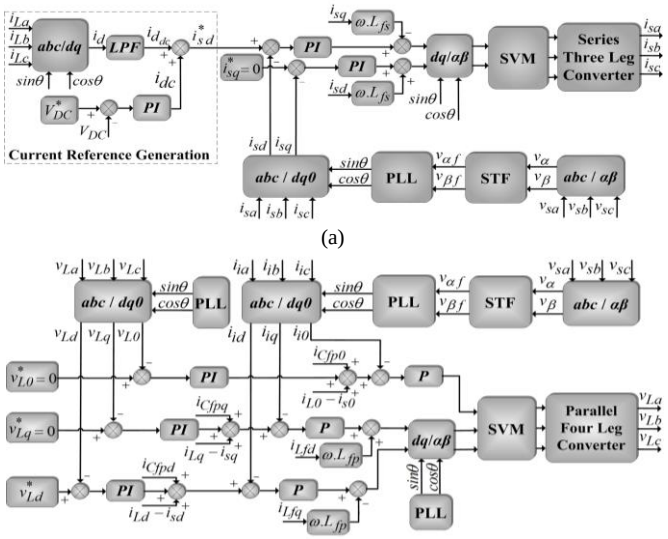
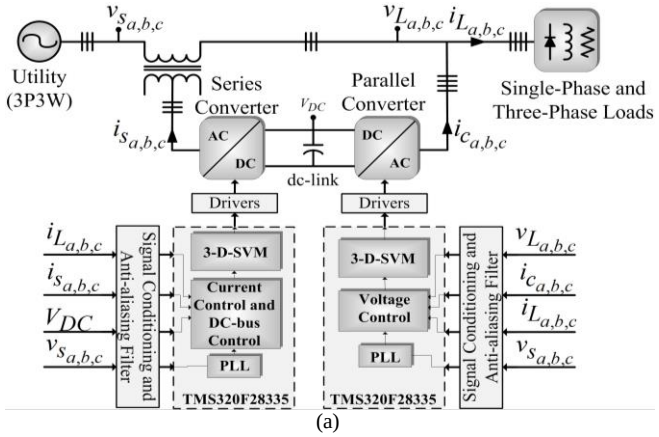
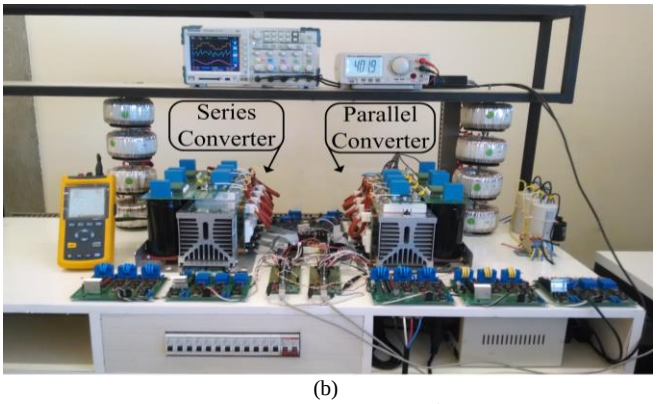


Fig. 5. Signal flow graphs of the reference generation and control scheme of both series and parallel PWM converters: (a) Reference current generation and the input current controllers; (b) Output voltage controllers.



(a)



(b)

Fig. 6. UPQC implementation: (a) schematic of the experimental setup; (b) experimental prototype.

The reference current of the quadrature axis q (i_{sq}^*) and i_{s0}^* are set to zero since the series converter synthesizes only positive sequence components (active currents), such that sinusoidal and balanced currents are achieved.

B. Parallel Converter Reference Voltages

The voltage control loop of the parallel converter is shown in the signal flow graph of Fig. 5(b). The reference voltage in the SRF direct axis d is defined by v_{Ld}^*. Its constant and continuous value represents the AC voltages (v_{La}, v_{Lb}, v_{Lc}) provided to the load. The reference voltages of the quadrature axis q (v_{Lq}^*) and v_{L0}^* are set to zero since sinusoidal and balanced voltages are desirable. As can be noted, the 3-D-SVM technique is employed in the parallel converter.

VI. Experimental Results

The performance of the implemented UPQC is evaluated by means of experimental tests based on the prototype shown in Fig. 6. Two digital signal processors (DSP TMS320F28335) were used for digital implementation of the SRF and PLL algorithms, as well as the PI controllers. IGBT modules (SK40GB 123 Semikron) with their respective drivers compose the 4-Leg converters. The main parameters used in the experimental tests are shown in Table I, whereas the controller parameters, such as the phase-margins and crossover frequencies used to determine the PI controller gains are shown in Table II. The controllers were tuned based on the frequency response method adopting the gain crossover frequency at 0dB and the phase-margin as design parameters [19]. Finally, the three-phase non-linear loads adopted in the experiments are described in Table III.

Fig. 7 presents the static behavior of the currents involved in the UPQC operation, considering the loads presented in Table III. The unbalanced load currents (i_{La}, i_{Lb}, i_{Lc}, i_{Ln}), the compensated source currents (i_{sa}, i_{sb}, and i_{sc}), and the compensation currents (i_{ca}, i_{cb}, i_{cc}, i_{cn}) are shown in Fig. 7(a), considering the unbalanced three-phase load (1). As can be noted, the source currents are sinusoidal, balanced, and with very low harmonic contents. In addition, it can be seen that the load neutral wire current (i_{Ln}) flows to the fourth leg of the parallel 4-Leg converter (i_{cn}). In Fig. 7(b) the experimental results for the unbalanced three-phase load (2) are shown, where the load currents (i_{La}, i_{Lb}, i_{Lc}), the currents related to phase "a" (i_{La}, i_{ca}, i_{sa}), and the input and output currents and voltages related to phase "a" (v_{sa}, i_{sa}, v_{La}, and i_{La}) can be seen. It can be noted that both the input currents, as well the output voltages are controlled to be in phase with the utility voltages.

The results obtained for the balanced three-phase load (1) are presented in Fig. 7(c), where the load currents (i_{La}, i_{Lb}, and i_{Lc}), the output voltage (v_{La}), the parallel converter compensation currents (i_{ca}, i_{cb} and i_{cc}), and the balanced source currents (i_{sa}, i_{sb} and i_{sc}) are shown.

The results presented in Fig. 7 show the ability of the UPQC to perform the power-line compensation even when only a 3P3W system is available at a plant site is, and the installed loads require a neutral conductor for connecting one or more single-phase loads (3P4W).

Table IV shows the THD of the load currents (i_{La}, i_{Lb}, i_{Lc}) and source currents (i_{sa}, i_{sb}, i_{sc}), where a significant reduction in the THDs related to the compensated source currents is noted.

Fig. 8 presents the static behavior of the voltages involved in the UPQC operation. Balanced, however distorted, input voltages (v_{sa}, v_{sb}, and v_{sc}), the compensated output voltages (v_{La}, v_{Lb} and v_{Lc}), and the compensation voltages across the

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series transformers (v_{Ca}, v_{Cb} and v_{Cc}) are shown in Fig. 8(a), whereas unbalanced, however undistorted, input voltages, the compensated output voltages, and the compensation voltages across the series transformers (v_{Ca}, v_{Cb} and v_{Cc}) are shown in Fig. 8(b), considering the unbalanced three-phase load (1). As can be seen, in both cases, the parallel converter provides sinusoidal, balanced, and regulated output voltages for the loads, with low harmonic contents. Since the output voltages are controlled to be sinusoidal, the series compensation voltages (v_{Ca}, v_{Cb} and v_{Cc}) are the difference between the input voltages and the output voltages. This means that the utility voltage harmonics, and/or voltage unbalances are indirectly compensated and naturally absorbed by the series transformers, without the need to use any method to calculate the compensation references. Table V presents the THD of the input and output voltages related to the experimental tests presented in Fig. 8(a). A significant reduction of the harmonic contents present in the output voltages is noted.

Fig. 9 presents the dynamic behavior of the DC-bus voltage (V_{DC}) and the source currents (i_{sa}, i_{sb}, and i_{sc}) when the load of phase "a" is disconnected and reconnected after a few seconds. Fig.9(a) presents the DC-bus voltage and the unbalanced load currents (i_{La}, i_{Lb}, i_{Lc}). As can be noted, even before and after the load transients, the source currents remain balanced as shown in Fig. 9(b). Fig. 9(c) shows the source currents in detail after the first transient. The action of the DC-bus voltage controller on the input currents keeps the voltage controlled at 400 V. The UPQC dynamic behavior under voltage sag (30%) during ten utility cycles is presented in Fig. 10 considering phase 'a'. As can be seen, the UPQC output voltage does not suffer with the voltage sag disturbance, remaining sinusoidal and regulated.

TABLE I
PARAMETERS USED IN THE TESTS CARRIED OUT ON THE UPQC

Apparent power of the unbalanced three-phase load (1)	S_a = 1590 VA, S_b = 1260 VA, S_c = 950 VA
Apparent power of the unbalanced three-phase load (2)	S_{La} = 1940 VA, S_{Lb} = 1260 VA, S_{Lc} = 1590 VA
Apparent power of the three-phase load	S_L = 4170 VA
Effective nominal voltage of the utility (line-to-neutral))	$V_{sa,b,c}$ = 127 V
Nominal utility grid frequency	f_s = 60 Hz
Switching frequency of the converters	f_{ch} = 20 kHz
Coupling inductance of the parallel converter	$L_{fpa,b,c}$ = 1.0 mH
Series resistance of the coupling inductors (parallel converter)	$R_{Lfpa,b,c}$ = 0.12 Ω
Capacitances of the parallel filters	$C_{fpa,b,c}$ = 85 μF
Coupling inductance of the series converter	$L_{fsa,b,c}$ = 1.5 mH
Series resistance of the coupling inductors (series converter)	$R_{Lfa,b,c}$ = 0.15 Ω
Dispersion inductance of the series coupling transformer	L_{dt} = 0.42 mH
Resistances of the series coupling transformers	$R_{ta,b,c}$ = 0.26 Ω
Transformation ratio of the series coupling transformers	n = 1
DC-bus voltage	V_{dc} = 400 V
DC-bus capacitance	C_{dc} = 9400 μF
DSP sampling frequency	f_a = 40 kHz
Gain of the PWM modulator	K_{PWM} = 2.66.10^{-4}

TABLE II
GAINS OF THE PI CONTROLLERS AND DESIGN SPECIFICATIONS

	Parallel Converter			Series Converter	
dq0-axes	Outer Loop		Inner Loop	Kp_s	Ki_s
	Kp_p	Ki_p	Kp_{pi}		
dq	0.2333 Ω^{-1}	549 Ω^{-1}/s	90 Ω	233.10 Ω	1217639 Ω/s
0	0.2381 Ω^{-1}	526 Ω^{-1}/s	361 Ω	---	---
DC-bus voltage				Kp_{dc}= 0.0357 Ω^{-1}	Ki_{dc}= 0.1202 Ω^{-1}/s
Crossover frequency of the parallel converter inner current loop				$\omega_{ci_p} = 2\pi f_s/6\ rad/s$	
Phase margin				MF_{ip}= 75°	
Crossover frequency of the parallel converter outer loop voltage				$\omega_{cv_p} = 0.16\omega_{ci_p}\ rad/s$	
Phase margin				MF_{vp}= 55°	
Crossover frequency of the series converter current loop				$\omega_{ci_s} = 2\pi f_s/9\ rad/s$	
Phase margin				MF_{is}= 50°	
Crossover frequency of the DC bus loop voltage				$\omega_{cv_{cc}} = 42\ rad/s$	
Phase margin				$MF_{v_{cc}}$= 87.5°	

TABLE III
LOAD PARAMETERS USED IN THE EXPERIMENTAL TESTS

Unbalanced three-phase loads		Phase A	Phase B	Phase C
Three single-phase full wave rectifiers	(1)	R=8.1 Ω L=380 mH	R=10.12 Ω L=346 mH	R=13.50 Ω L=357 mH
	(2)	R=13.5 Ω C=940 μF	R=10.12 Ω L=346 mH	R=8.1 Ω L=380 mH
Balanced three-phase load		Phases ABC		
Three-phase full wave rectifier	(1)	R=17.7 Ω		

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TABLE IV
LOAD AND SOURCE CURRENTS TOTAL HARMONIC DISTORTIONS

Three-phase loads	Total Harmonic Distortion (THD %)					
	i_{La}	i_{Lb}	i_{Lc}	i_{sa}	i_{sb}	i_{sc}
Unbalanced three-phase load (1)	30.7	25.0	24.9	1.2	1.0	1.0
Unbalanced three-phase load (2)	62.7	25.0	30.7	0.9	1.0	1.2
Three-phase load (1)	26.0	26.0	26.0	1.7	1.7	1.7

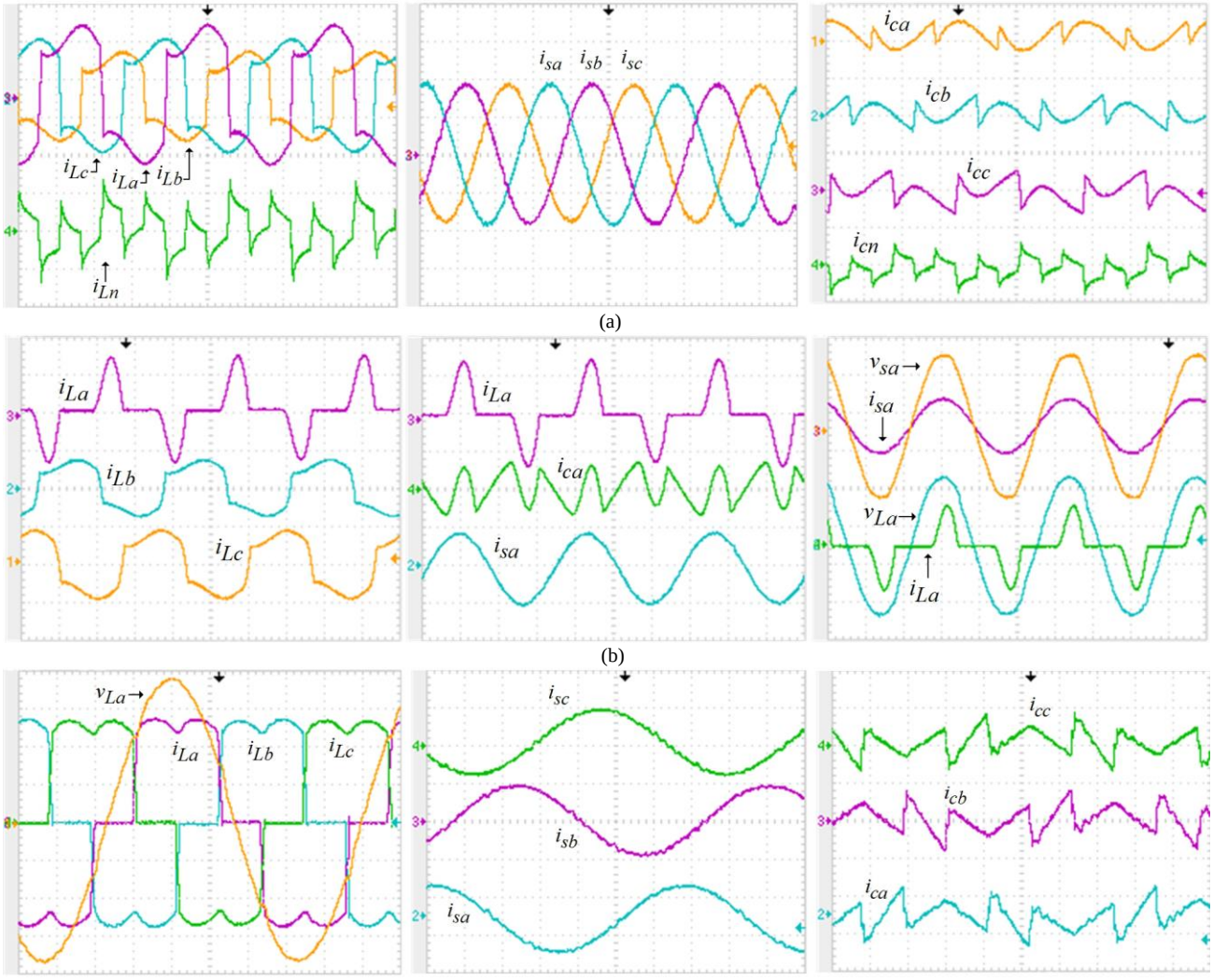

Fig. 7. Experimental results for the loads presented in Table III: (a) UPQC currents for unbalanced three-phase -phase load (1) (20 A/div, 5 ms/div): Load currents (i_{La}, i_{Lb}, i_{Lc}) and i_{Ln}, Compensated source currents (i_{sa}, i_{sb}, i_{sc}), and Currents of the parallel converter (i_{ca}, i_{cb}, i_{cc}) and i_{cn}; (b) Currents and voltages of phase "a" of the UPQC for the unbalanced three-phase load (2) (20 A/div, 100V/div, 5 ms/div): Load currents (i_{La}, i_{Lb}, i_{Lc}); Currents of phase "a": load i_{La}, parallel converter i_{ca} and source i_{sa}; voltages and currents of phase "a": load current i_{La} , source current i_{sa}, utility voltage v_{sa} and load voltage v_{La}, (c) UPQC currents for three-phase load (1) (2.5 ms/div): Load currents (i_{La}, i_{Lb}, i_{Lc}) (5 A/div), Source compensated currents (i_{sa}, i_{sb}, i_{sc}) (10 A/div), Parallel converter currents (i_{ca}, i_{cb}, i_{cc}) (10 A/div).

TABLE V
THD OF THE INPUT AND OUTPUT VOLTAGES FOR THE UNBALANCED THREE-PHASE LOAD (1)

Three-phase load	Total Harmonic Distortion (THD%)					
	v_{sa}	v_{sb}	v_{sc}	v_{La}	v_{Lb}	v_{Lc}
Unbalanced three-phase load (1)	12.3	12.3	12.3	1.8	1.7	1.7

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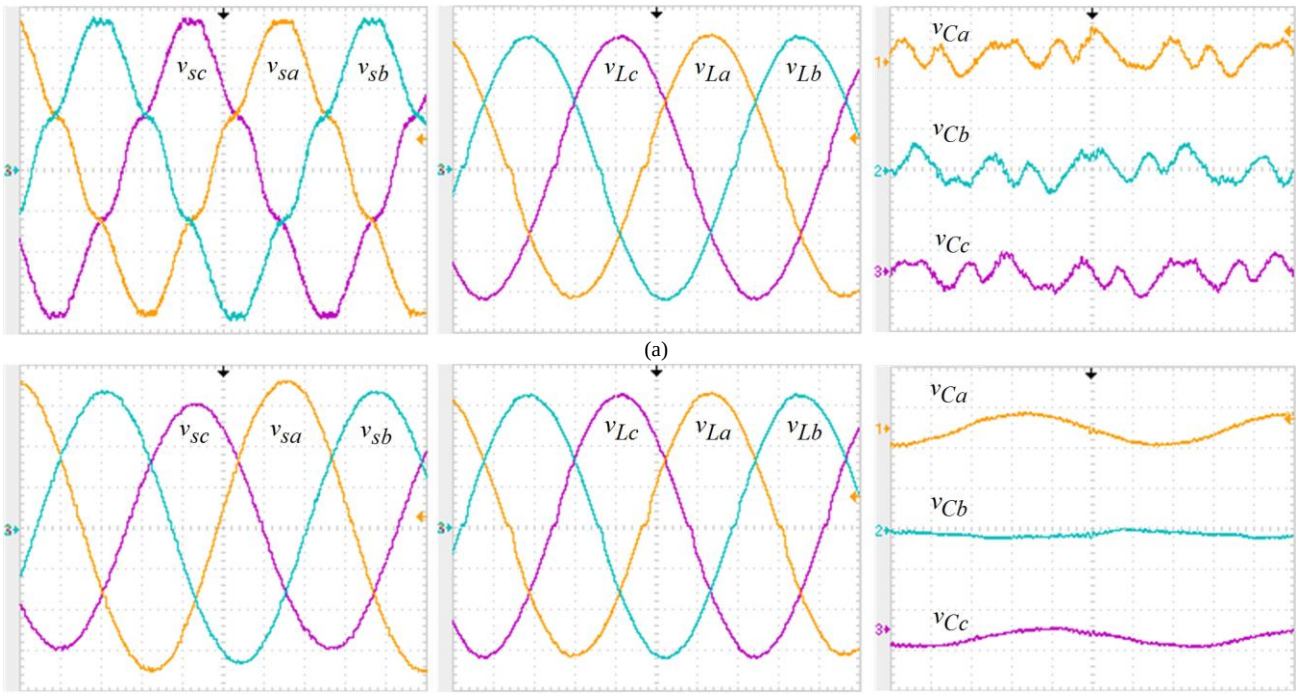

Fig. 8. Voltages of the UPQC under utility harmonics and unbalances for the unbalanced three-phase load (1): (a) Utility voltages (v_{sa}, v_{sb}, v_{sc}) (50 V/div, 2,5ms/div), Load voltages (v_{La}, v_{Lb}, v_{sL}) (50 V/div, 2,5ms/div) and series compensating voltages (v_{Ca}, v_{Cb} and v_{Cc}) (50 V/div, 2,5ms/div); (b) (a) Utility voltages (v_{sa}, v_{sb}, v_{sc}) (50 V/div, 2,5ms/div), Load voltages (v_{La}, v_{Lb}, v_{sL}) (50 V/div, 2,5ms/div) and series compensating voltages (v_{Ca}, v_{Cb} and v_{Cc}) (50 V/div, 2,5ms/div)

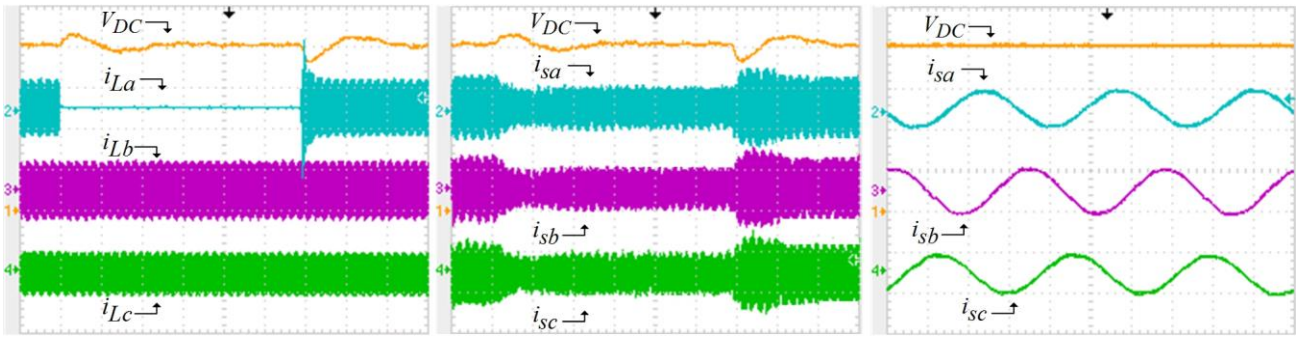

Fig. 9. Voltages and current of the UPQC for the unbalanced three-phase load 1: (a) DC-bus voltage (V_{DC}) (100 V/div, 500ms/div) and load currents (i_{La}, i_{Lb}, i_{Lc}) (20 A/div, 500ms/div); (b) DC-bus voltage (V_{DC}) (100 V/div, 500ms/div) and source currents (i_{sa}, i_{sb}, i_{sc}) (20 A/div, 500ms/div); (c) DC-bus voltage (V_{DC}) (100 V/div, 5ms/div) and details of the source currents (i_{sa}, i_{sb}, i_{sc}) after the first load transient (20 A/div, 5ms/div).

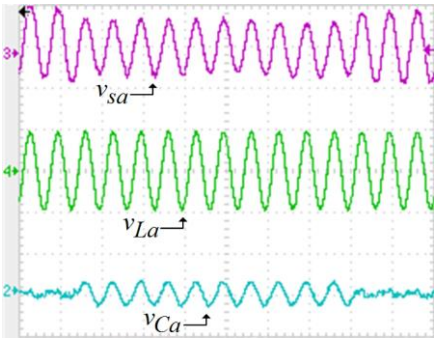

Fig. 10. UPQC under voltage sag disturbance (phase 'a'): utility voltage (v_{sa}), load voltage (v_{La}) and series compensating voltage (v_{Ca}) (200 V/div, 25ms/div).

Harmonic spectra and the THDs related to the input and output voltages and currents of the UPQC are presented in Fig. 11. The THDs of the utility voltage (v_{sa}) and the load voltage (v_{La}) measured in phase 'a' are shown in Fig. 11(a), whereas the THDs of the source current (i_{sa}) and the load current (i_{La}) are shown in Fig. 11(b) for the unbalanced three-phase load (1). The current harmonic spectra and THDs of the UPQC supplying the unbalanced three-phase load (2), measured in phase 'a' (i_{sa}, i_{La}), are shown in Fig. 11(c).

VII. Conclusion

This paper presents a practical and versatile application based on UPQC, which can be used in three-phase three-wire (3P3W), as well as three-phase four-wire (3P4W) distribution systems. It was demonstrated that the UPQC installed at a 3P3W system plant site was able to perform universal active filtering even when the installed loads required a neutral conductor for connecting one or more single-phase loads

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(3P4W). The series-parallel active filtering allowed balanced and sinusoidal input currents, as well as balanced, sinusoidal and regulated output voltages.

By using a dual control compensating strategy, the controlled voltage and current quantities are always sinusoidal. Therefore, it is possible to reduce the complexity of the algorithms used to calculate the compensation references. Furthermore, since voltage and current SRF-based controllers are employed, the control references become continuous, reducing the steady-state errors when conventional PI controllers are used.

Based on digital signal processing and by means of extensive experimental tests, static and dynamic performances, as well as the effectiveness of the dual UPQC were evaluated, validating the theoretical development.

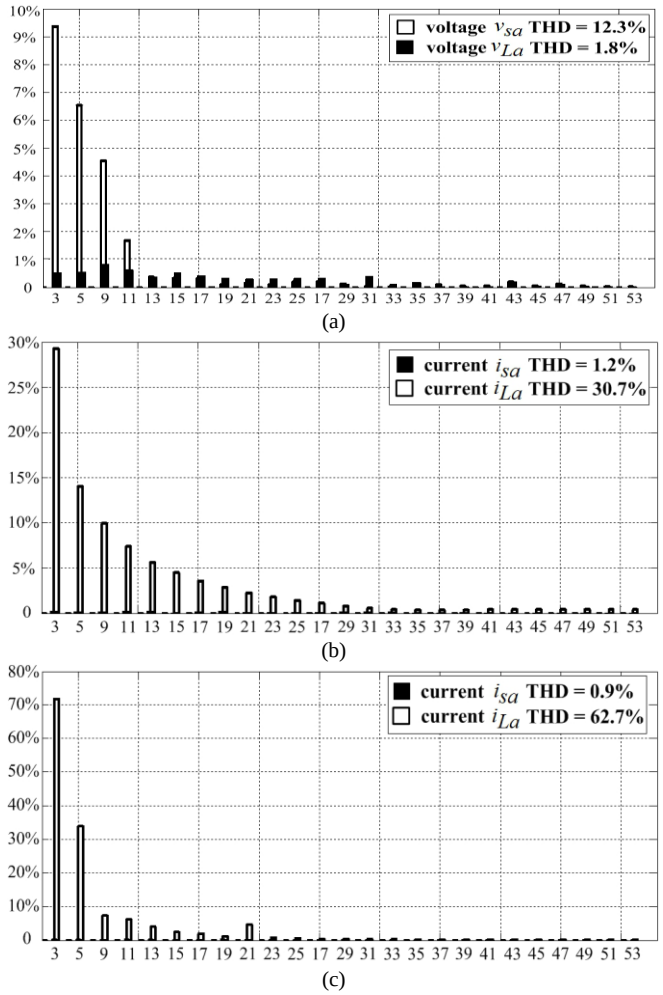

Fig. 11. Harmonic spectra and THDs of voltage and current. (a) voltages of phase "a" for the unbalanced three-phase load 1: utility voltage v_{sa} and load voltage v_{La}; (b) currents of phase "a" for the unbalanced three-phase load 1: source current i_{sa} and load current i_{La}; (c) currents of phase "a" for the unbalanced three-phase load 2: source current i_{sa} and load current i_{La}.

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